What is claimed is:

1. A tester for interposing between first and second logic, wherein the first logic and second logic have respective first and second logic output drivers and the tester is operable in test cycles to periodically test for contention between the logic drivers, dynamic contention being detected responsive to a signal asserted by the first logic driver during one of the test cycles, and a signal asserted by the second logic driver during an immediately succeeding one of the test cycles, and static contention being detected responsive to a signal asserted by the first logic driver during one of the test cycles and a signal asserted by the second logic driver during the same one of the test cycles.

2. A tester for interposing between first and second logic, wherein the first logic and second logic are capable of operating at respective specified operating frequencies and have respective first and second logic output drivers, the tester being operable with the first and second logic in test cycles, at a test frequency lower than the specified operating frequencies, to periodically test for contention between the logic drivers, wherein during a first interval of such a test cycle, beginning after the logic drivers have driven respective driver signals, the tester is operable to isolate the respective first and second logic from one another to detect the logic driver signals, and during a second interval, following the first interval, the tester is operable to permit data transfer between the first and second logic.

3. The tester of claim 2, wherein the testing for contention includes detecting dynamic contention responsive to a signal asserted by the first logic driver during one of the test cycles,

and a signal asserted by the second logic driver during an immediately succeeding one of the test cycles.

4. The tester of claim 2, wherein the testing for contention includes detecting static contention responsive to a signal asserted by the first logic driver during one of the test cycles and a signal asserted by the second logic driver during the same one of the test cycles.

5. A tester for interposing between first and second logic, wherein the first logic and second logic have respective first and second output drivers and the tester is operable in test cycles to periodically test for contention between the drivers, the tester comprising:

tester logic;

a first tester node for coupling to the first logic driver;

a second tester node for coupling to the second logic driver;

a switch coupled to the first and tester second nodes, wherein the tester logic is operatively coupled to the switch and operable to open the switch during a certain interval of the test periods, so that the respective first and second logic are electrically decoupled from one another by the open switch during the certain interval;

a first test receiver coupled to the first tester node and to the tester logic for sensing a signal on the first node; and

a second test receiver coupled to the tester second node and to the tester logic for sensing a signal on the second node, wherein the periodic testing for contention includes signals of the logic output drivers during the certain interval being registered by the tester logic responsive to the respective test receivers.

6. The tester of claim 5, comprising:

a first test source coupled to the first tester node for asserting and de-asserting signals on the first node during one portion of the certain interval responsive to the tester logic; and

a second test source coupled to the second tester node for asserting and de-asserting signals on the second node during another portion of the certain interval responsive to the tester logic, wherein the test receivers sense the logic driver signals during the certain interval responsive to the test source signals.

7. The tester of claim 6, wherein the periodic testing for contention includes the tester logic detecting dynamic contention responsive to a signal asserted by the first logic driver during one of the test cycles, and a signal asserted by the second logic driver during an immediately succeeding one of the test cycles.

8. The tester of claim 6, wherein the periodic testing for contention includes the tester logic detecting static contention responsive to a signal asserted by the first logic driver during one of the test cycles and a signal asserted by the second logic driver during the same one of the test cycles.

9. A method for testing, comprising the steps of:

interposing a tester between first and second logic, wherein the first logic and second logic have respective first and second output drivers;

operating the tester in test cycles;

detecting dynamic contention responsive to a signal asserted by the first driver during one of the test cycles and a signal asserted by the second driver during an immediately succeeding one of the test cycles; and

detecting static contention responsive to a signal asserted by the first driver during one of the test cycles and a signal asserted by the second driver during the same one of the test cycles.

10. A method for testing, comprising the steps of:

interposing a tester between first and second logic, wherein the first logic and second logic are capable of operating at respective specified operating frequencies and have respective first and second output drivers; and

operating the tester and the first and second logic in test cycles, at a test frequency lower than the specified operating frequencies, to periodically test for contention between the drivers, wherein the periodic testing for contention comprises the steps of:

decoupling the respective first and second logic from one another by the tester during a first interval of such a test cycle, the first interval beginning after the drivers have driven respective driver signals;

detecting the driver signals by the tester during the first interval; and

recoupling the respective first and second logic drivers to one another by the tester during a second interval, following the first interval, to permit data transfer between the first and second logic.

11. The method of testing of claim 10, wherein the periodic testing for contention comprises the steps of:

detecting dynamic contention responsive to a signal asserted by the first driver during one of the test cycles, and a signal asserted by the second driver during an immediately succeeding one of the test cycles.

12. The method of testing of claim 10, wherein the periodic testing for contention comprises the steps of:

detecting static contention responsive to a signal asserted by the first driver during one of the test cycles and a signal asserted by the second driver during the same one of the test cycles.

13. A method for testing, comprising the steps of:

interposing a tester between first and second logic, wherein the first logic and second logic have respective first and second output drivers, wherein a first tester node is coupled to the first logic driver, a second tester node is coupled to the second logic driver, and a tester switch is coupled to the first and tester second nodes; and

operating the tester in test cycles to periodically test for contention between the drivers, wherein the periodic testing comprises the steps of:

decoupling the respective first and second logic from one another by opening the tester switch during a certain interval of the test cycles;

sensing a signal on the first tester node by a first test receiver during the certain interval; and

sensing a signal on the second tester node by a second test receiver during the certain interval, wherein the logic driver signals are detected responsive to the tester node sensing.

14. The method of claim 13, wherein detecting logic driver signals comprises the steps of:

asserting signals by respective first and second test sources coupled to the tester nodes and registering respective tester node signals sensed by the respective test receivers during one portion of the certain interval;

de-asserting signals by the respective first and second test sources and registering respective tester node signals sensed by the respective test receivers during another portion of the certain interval; and

determining the signals driven by the logic driver signals responsive to the registered tester node signals.

15. The method of claim 14, wherein the periodic testing for contention comprises the step of:

detecting dynamic contention responsive to a signal asserted by the first logic driver during one of the test cycles, and a signal asserted by the second logic driver during an immediately succeeding one of the test cycles.

16. The method of claim 14, wherein the periodic testing for contention comprises the step of:

detecting static contention responsive to a signal asserted by the first logic driver during one of the test cycles and a signal asserted by the second logic driver during the same one of the test cycles.

17. A computer program product for testing, comprising:

instructions for operating a tester in test cycles, wherein the tester is interposed between first and second logic, and the first logic and second logic have respective first and second output drivers;

instructions for detecting dynamic contention responsive to a signal asserted by the first driver during one of the test cycles and a signal asserted by the second driver during an immediately succeeding one of the test cycles; and

instructions for detecting static contention responsive to a signal asserted by the first driver during one of the test cycles and a signal asserted by the second driver during the same one of the test cycles.

18. A computer program product for testing first and second logic, wherein the first logic and second logic are capable of operating at respective specified operating frequencies and have respective first and second logic output drivers, the computer program product comprising:

first instructions for operating a tester in test cycles, at a test frequency lower than the specified operating frequencies, to periodically test for contention between the logic drivers, wherein the first instructions comprise:

second instructions for decoupling the respective first and second logic from one another by the tester during a first interval of such a test cycle, the first interval beginning after the drivers have driven respective driver signals;

third instructions for detecting the driver signals by the tester during the first interval; and

fourth instructions for recoupling the respective first and second logic drivers to one another by the tester during a second interval, following the first interval, to permit data transfer between the first and second logic.

19. The computer program product of claim 18, wherein the first instructions comprise:

instructions for detecting dynamic contention responsive to a signal asserted by the first driver during one of the test cycles, and a signal asserted by the second driver during an immediately succeeding one of the test cycles.

20. The computer program product of claim 18, wherein the first instructions comprise:

instructions for detecting static contention responsive to a signal asserted by the first driver during one of the test cycles and a signal asserted by the second driver during the same one of the test cycles.

21. The computer program product of claim 18, wherein the third instructions comprise:

instructions for decoupling the respective first and second logic from one another by causing a switch of the tester to open during a certain interval of the test cycles;

instructions for sensing a signal on a first node of the tester by a first receiver of the tester during the certain interval; and

instructions for sensing a signal on a second node of the tester by a second receiver of the tester during the certain interval, wherein the logic driver signals are detected responsive to the tester node sensing.

22. The computer program product of claim 13, wherein instructions for the detecting of the logic driver signals comprise:

instructions for i) asserting signals by respective first and second test sources of the tester coupled to the tester nodes, and ii) registering respective tester node signals sensed by the respective test receivers during one portion of the certain interval;

instructions for i) de-asserting signals by the respective first and second test sources, and ii) registering respective tester node signals sensed by the respective test receivers during another portion of the certain interval; and

instructions for detecting the signals driven by the logic drivers responsive to the registered tester node signals.